



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,116	10/31/2003	Kevin Donnelly	60809-0143-US	4990

7590 01/21/2005

MORGAN LEWIS & BOCKIUS  
2 PALO ALTO SQUARE  
3000 EL CAMINO REAL  
SUITE 900  
PALO ALTO, CA 94306

EXAMINER
----------

CHACE, CHRISTIAN

ART UNIT	PAPER NUMBER
----------	--------------

2187

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/699,116

Applicant(s)

DONNELLY ET AL.

Examiner

Christian P. Chace

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 November 2004.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-32 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☒ Claim(s) 1-10, 13-16, 22, 23 and 27-32 is/are allowed.  
6) ☒ Claim(s) 11, 12, 17-21 and 24-26 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 31 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 11/15/04, 12/14/04.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Amendment***

This Office action has been issued in response to amendment filed 15 November 2004. Claims 1-32 are pending. Claims 1-10, 13-16, 22-23, and 27-32 are allowed. Claims 11-12, 17-21, and 24-26 are rejected. Applicants' arguments have been carefully and respectfully considered in light of the instant amendment, but they are not entirely persuasive. Accordingly, this action has been made FINAL, as necessitated by amendment.

### ***Information Disclosure Statement***

IDSs submitted 15 November and 14 December 2004 have been considered by examiner. Signed and initialed copies are attached hereto.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11-12, 17-20, and 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Capowski et al US Patent #5,513,377 and Microsoft Press Computer Dictionary (MPCD), offered as extrinsic evidence.

With respect to independent claim 11, a system is disclosed in the abstract.

A first channel is disclosed in figure 1, as STI Bus 16, in the upper half of the figure.

A second channel is disclosed in figure 1 as STI Bus 16, in the lower half of the figure.

A first device coupled the first channel is disclosed in figure 1 as side A logic.

A second device coupled to the second channel is disclosed in figure 1 as side B logic.

A transceiver having latency aligning circuitry coupled to the first channel and the second channel is disclosed as STI receive logical macros #28. It is important to note that "latency aligning circuitry" is discussed in the specification at page 5, paragraph 28 as circuitry that adjusts transfer latency from the host channel to the stick channel according to the phase difference between host clocks. While this discusses what the circuitry does, it does not disclose what it is, specifically, e.g., the physical make-up of the device. Accordingly, examiner is left to assume that the physical make-up must be within the scope of what the ordinary artisan would recognize without undue experimentation (otherwise, there would be a 235 USC 112, 1<sup>st</sup> Paragraph issue). Therefore, examiner has interpreted the claimed device in light of the disclosure, which is merely a recitation of what the circuitry does as described in the specification. Accordingly, the discussion of the receive logical macros in column 4, lines 52-60 discusses the alignment of phases between devices.

The first and second channels being bi-directional communication channels is disclosed in figure 1 of Capowski et al as STI bus #16 (both top and bottom), a first and second of which are show in figure 5, and further discussed at column7, line 57 into column 8line 15. A bus is defined by MPCD, for example, as, "a SET (emphasis added)

of hardware lines..." A channel is a bus. "Bi-directional" is defined by MPD, for example, as "operating in two directions," "a bi-directional bus can transfer signals in both directions between two devices," as shown in figure 1, for each bus #16.

With respect to claim 12, at least one of the first and second channels being a serial link is disclosed in column 4, lines 44-47.

With respect to claim 17, the transceiver further comprising isolation logic (again, the specification only discusses what it does, not specifically what it is) to prevent retransmission of data received from the second channel, to the second channel, is disclosed in figure 1 as STI macros, which clearly have arrows either going in or coming out of each one, thereby ensuring no retransmission in the other direction.

With respect to claim 18, the transceiver further comprising latch-up prevention logic to prevent feedback of data between the first and second channels could be interpreted in the same manner as above with respect to claim 17 – examiner is unsure what the difference in the instantly claimed invention is between "retransmission" and "feedback."

With respect to claim 19, the transceiver further comprising a first synchronizing unit that synchronizes data transmitted from the first channel to the second channel is disclosed in figure 1 as synch buffer #22 on the A side of the figure.

With respect to claim 20, the transceiver further comprising a second synchronizing unit that synchronizes data transmitted from the second channel to the first channel is disclosed in figure 1 as synch buffer #22 on the B side of the figure.

With respect to independent claim 25, a memory system is disclosed in column 1, line 57, for example.

A memory controller coupled to a primary channel is disclosed in figure 1 as side A logic, which, as discussed in column 4, lines 24-27, may be any one of a variety of components, including a memory controller.

A first transceiver, having latency alignment circuitry (as discussed supra with respect to claim 11), coupled to primary channel and to a first stick channel is disclosed in figure 1 as #18 and 322, on side A of the figure.

A first memory device having a programmable delay coupled to the first stick channel is disclosed as synch buffer #22, on the B side of figure 1, at the top of the figure.

A second memory device having a programmable delay coupled to the primary channel or the first stick channel is disclosed as the synch buffer #22, on the B side, on the bottom half of figure 1.

The primary and first stick channels being bi-directional communication channels is disclosed in figure 1 of Capowski et al as STI bus #16 (both top and bottom), a first and second of which are show in figure 5, and further discussed at column 7, line 57 into column 8, line 15. A bus is defined by MPCD, for example, as, "a SET (emphasis added) of hardware lines..." A channel is a bus. "Bi-directional" is defined by MPCD, for example, as "operating in two directions," "a bi-directional bus can transfer signals in both directions between two devices," as shown in figure 1, for each bus #16.

With respect to claim 26, a second transceiver having latency aligning circuitry coupled to the stick channel and a second stick channel is disclosed in figure 1 as STI Transmit and Receive logic, on the B side of the figure.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Capowski et al (cited supra) and MPCD (extrinsic evidence – cited supra).

With respect to claim 21 Capowski et al and MPCD disclose the subject matter claimed in the claims upon which the instant claim depends.

The difference between the instant claims and Capowski et al and MPCD is the explicit recitation of power logic that turns off the transceiver when the transceiver does not need to transmit.

Capowski et al disclose that the power required for distance impede I/O element miniaturization, in column 2, lines 30-33, therefore disclosing the desirability to reduce power needs in the system.

Turning an element off reduces power consumption. Examiner takes OFFICIAL NOTICE of this teaching.

Accordingly, it would have been obvious to one of ordinary skill in the art, having the teachings of Capowski et al and MPCD before him/her at the time of the invention,

to turn off elements in the system that aren't being used, in order to reduce power consumption, as discussed supra.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Capowski et al (cited supra) and MPCD (extrinsic evidence – cited supra) in view of Li (US Patent Application Publication #2004/0095838).

With respect to claim 24, Capowski et al and MPCD disclose the subject matter claimed in the claims upon which the instant claims depend. Capowski et al also disclose synchronizing circuitry other than the buffers of figure 1, for bit synchronization, in column 4, line 66 into column 5, line 13.

The difference between the instant claim and Capowski et al and MPCD is the transceiver comprising at least one phase locked loop that performs clock recovery.

Li discloses a phase locked loop that performs "clock recovery," or synchronization, in paragraph 9 as a delay locked loop.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Capowski et al and MPCD and Li before him/her, to utilize the delay locked loop of Li in the system of Capowski et al to produce a synchronized clock signal for proper access to the memory, as also disclosed in paragraph 9 of Li.

### ***Response to Arguments***

With respect to applicants' arguments that Capowski et al do not teach the channels being bi-directional, examiner respectfully disagrees, and has included, as extrinsic evidence, definitions of "bi-directional" and "bus."



With respect to applicants' argument that there is no motivation for one skilled in the art, according to the teachings of Capowski et al, to design a system that turns off any I/O element for the purpose of reducing power usage. Examiner respectfully disagrees. As noted in the rejection supra, power required for distance impedes miniaturization – accordingly, by reducing the power needed, and the elements may then be miniaturized. However, even assuming, *arguendo*, applicants' arguments were persuasive, reducing power consumption in and of itself is so desirable for so many reasons in the computer accessing and control art, so as to make it hackneyed.

With respect to applicants' argument that Li does not disclose or suggest that the memory device comprises two bi-directional communication channels that are coupled to a transceiver having latency aligning circuitry, examiner notes that this is not what Li was used for the rejection, and, therefore, the argument is not commensurate with the rejection, in light of the revised rejection of claim 11, upon which claim 24 depends.

***Allowable Subject Matter***

Claims 1-10, 13-16, 22-23, and 27-32 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to independent claim 1, a re-timer configured to re-time data received from the first channel using the first clock signal and to retransmit the data to the second channel using the fourth clock signal, based on the definition of the re-timer in the instant specification at paragraph 56 on page 13, is not taught or suggested by

Art Unit: 2187

the currently cited prior art of record. Claims 2-10 depend upon the instant claim and are allowable for at least the reasons set forth supra with respect to same.

With respect to now independent claims 13, 14, and 27, the record is clear as to their respective reasons for allowability. Claims 22-23, 15-16, and 28-32 depend upon the instant claims, respectively, and are allowed for at least the reasons set forth supra with respect to same.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

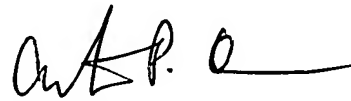
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 571.272.4190. The examiner can normally be reached on MAXI FLEX.

Art Unit: 2187

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571.272.4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'C. P. Chace', with a long horizontal flourish extending to the right.

Christian P. Chace  
Examiner  
Art Unit 2187